

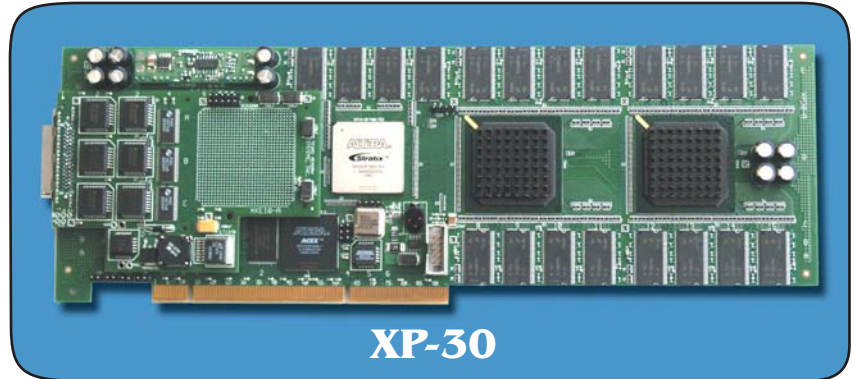
# XP-30

## 16 GFLOPS DSP Accelerator

Turn your Server into  
a DSP Supercomputer

### XP-30 Architecture

Based on the popular XP-15, the XP-30 integrates several functions within a single PCI card. The XP-30 includes two complete TM-44 DSP processing nodes, a separate global memory, an I/O daughter card, and the PCI interface. With the XKE-10 I/O daughter card, the XP-30 can input two ECL channels, preprocess this data through a high-density Xilinx FPGA, and store the results in global memory for additional processing with the two TM-44 DSP nodes. Users can now have the best of both worlds. TM-44 nodes will do the standard DSP processing and the Xilinx FPGA can do the special data manipulation functions (tune, filter, decimate). Central to the data flow within the XP-30 is the high-bandwidth (1.5 GB/sec) global memory that provides a high-speed buffer for all devices. The XP-30 eliminates most PCI data transfers usually associated with XP-15 operations. Now, only the final result needs to be transferred on the PCI-bus to the host computer's memory.



XP-30

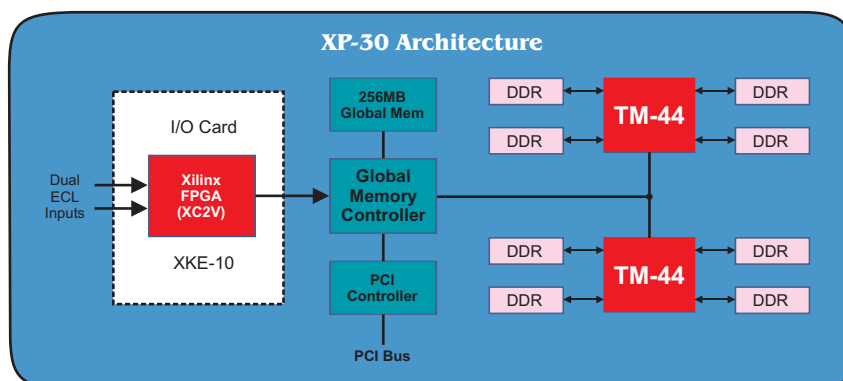
### TM-44 Architecture

The XP-30 is based on two TM-44 DSP nodes for most of its number crunching power. The TM-44 is a chip developed by Texas Memory Systems, Inc. to do intense DSP algorithms easily. The TM-44 chip is comprised of 80 floating point processing units running at 100 MHz, a high bandwidth external memory bus (**8.0 GB/sec**), four special elementary function units (trigonometric functions, square root, divide), and on-chip program memory. The TM-44 executes a very long instruction word (VLIW) program, processing multiple data values each clock cycle. Each TM-44 DSP node has **8 GFLOPS** of processing power, 8 GB/sec of memory bandwidth, and many additional units necessary to maintain processing efficiency.

### TM-44 Math Library

The TM-44 math library contains more than 500 scientific algorithms optimized to run efficiently on the TM-44 chip. Library coverage includes real and complex vector arithmetic and matrix arithmetic. It also includes 1-D and 2-D FFTs (powers of 2, 3 and 5 vector sizes), DSP and image processing algorithms, as well as re-sampling, tuning, data comparison, packing and binary arithmetic utilities. Also included are elementary function routines for executing trigonometric, square root, and division operations in a few nanoseconds instead of microseconds. Library documentation provides calling sequences, detailed algorithm descriptions, performance timings, and examples. Programming the TM-44 is as easy as calling a library function. XP-30 software is comprised of a driver to allow the host computer to talk to the PCI card and the math library of over 500 scientific algorithms.

The XP-30 allows users to turn their Servers quickly into DSP supercomputers.



### TM-44 Node

FFT - 64K complex	0.66 msec
FFT - 1024K complex	13.20 msec
1 million point Arctan2	2.63 msec
128K rectangular to polar	0.33 msec

[www.superDSP.com](http://www.superDSP.com)

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